REMARKS

In the Office Action, the Examiner noted that claims 1-24 are pending in the application and that claims 1-24 are rejected. By this response, claims 1, 17, and 24 are amended. In view of the above amendments and the following discussion, Applicants submit that none of the claims now pending in the application are anticipated under the provisions of 35 U.S.C. §102 or obvious under the provisions of 35 U.S.C. §103. Thus, Applicants believe that all of these claims are now in condition for allowance.

I. Objections

The Examiner objected to the specification, stating that the title should not be included in the abstract. (Office Action, p. 2). Applicants have amended the specification to remove the title from the Abstract section. Accordingly, Applicants respectfully request that the objection to the specification be withdrawn.

II. Rejection of Claims Under 35 U.S.C. §112

The Examiner has rejected claims 1-24 in the Office Action under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicants regard as the invention. The Examiner stated that the term "threads" is not clearly defined in the claims. (Office Action, p. 2). Applicants have amended claims 1, 17, and 24 to recite that each of the plurality of threads comprises a "concurrent execution unit." See Applicants' specification, paragraph [0093]. Applicants contend that claims 1-24, when read in light of the specification by one skilled in the art, are definite and fully comply with 35 U.S.C. §112, second paragraph. Accordingly, Applicants respectfully request that rejection of such claims be withdrawn.

III. Rejection of Claims Under 35 U.S.C. §102

The Examiner rejected claims 1-5, 8-9, 11, 13-21, and 24 as being anticipated by Davis et al. (U.S. Patent 6,230,307, issued May 8, 2001). More specifically, the Examiner stated that Davis teaches defining first attributes for a plurality of threads,

defining second attributes for a memory, defining third attributes for an interconnection topology associated with at least one of the memory and the plurality of threads, and defining fourth attributes for an interface to at least one of the memory and the plurality of threads. (Office Action, p. 3). The rejection is respectfully traversed.

Davis discloses a system for development and execution of reconfigurable hardware resources. (Davis, Abstract). The system includes a development environment and a runtime environment. (Davis, col. 6, lines 3-5). The development environment uses a library of hardware objects that are connected together using high-level software language constructs or "wrappers." (Davis, col. 8, lines 39-67; FIG. 9).

Davis does not teach each and every element of Applicants' invention recited in amended claim 1. Namely, Davis does not teach or suggest defining attributes for a memory for storing messages to be operated on by a plurality of threads. Davis discloses specification of hardware objects, which are analogized with software threads. Davis, however, does not disclose specification of a memory, in particular, a memory for storing messages to be operated on by threads or hardware objects. While Davis states "[f]or a hardware object, it is the state of all of the registers and memory elements inside of the design," this disclosure does not teach or suggest defining attributes for a memory for storing messages to be operated on by threads. (Davis, col. 9, lines 22-24). Rather, Davis is describing how a hardware object has state similar to a software thread. The development environment in Davis is not invoked to define attributes for a memory, as recited in Applicants' claim 1.

"Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim." Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 221 USPQ 481, 485 (Fed. Cir. 1984). Since Davis does not teach defining attributes for a memory for storing messages to be operated on by a plurality of threads, Davis does not teach each and every element of Applicant's claim 1 as arranged therein. In addition, since Davis does not teach defining attributes for a memory for storing messages to be operated on by a plurality of threads, Davis does not teach defining attributes for an interconnection topology associated with the memory or an interface to the memory. Accordingly, Davis does not anticipate Applicant's invention recited in claim 1.

Claims 17 and 24 include features similar to those emphasized above in claim 1. For the same reasons discussed above, Davis does not anticipate Applicants' invention recited in claims 17 and 24. Finally, claims 2-5, 8-9, 11, 13-16, and 18-21 depend, either directly or indirectly, from claims 1 and 17 and recite additional features therefor. Since Davis does not anticipate Applicants' invention as recited in claims 1 and 17, dependent claims 2-5, 8-9, 11, 13-16, and 18-21 are also not anticipated and are allowable. Therefore, Applicants contend that claims 1-5, 8-9, 11, 13-21, and 24 are not anticipated by Davis and, as such, fully satisfy the requirements of 35 U.S.C. §102. Applicants respectfully request that the rejection of such claims be withdrawn.

IV. Rejection Of Claims Under 35 U.S.C. §103

A. Claims 6-7 and 22-23

The Examiner rejected claims 6-7, and 22-23 as being unpatentable over Davis et al. in view of Davidson et al. (United States patent 6,671,869, issued December 30, 2003). The rejection is respectfully traversed.

Claims 6-7 and 22-23 depend from claims 1 and 17 and recite additional features therefor. The grounds of rejection for dependent claims 6-7 and 22-23 are predicated on the validity of the rejection under 35 U.S.C. §102 given Davis. As discussed above, Davis does not teach or suggest Applicants' invention recited in claims 1 and 17. Davidson discloses a graphical interface that allows a user to graphically define at least one type of input data unit that is expected to be received at a programmable circuit. (See Davidson, Abstract). Davidson does not teach or suggest that which is missing from Davis, namely, defining attributes for a memory for storing messages to be operated on by a plurality of threads. Applicants contend that no conceivable combination of the cited references renders obvious Applicants' claim 1. Therefore, claims 6-7 and 22-23, which depend from claims 1 and 17, are patentable over the combination of Davis and Davidson and, as such, fully satisfy the requirements of 35 U.S.C. §103. Accordingly, Applicants respectfully request that the rejection of such claims be withdrawn.

B. Claims 10 and 12

The Examiner rejected claims 10 and 12 as being unpatentable over Davis in view of Vandeweerd et al. (US published patent application 2004/0006584, published January 8, 2004). The rejection is respectfully traversed.

Claims 10 and 12 depend from claim 1 and recite additional features therefor. The grounds of rejection for dependent claims 10 and 12 are predicated on the validity of the rejection under 35 U.S.C. §102 given Davis. As discussed above, Davis does not teach or suggest Applicants' invention recited in claim 1. Vandeweerd discloses an array of parallel programmable processing engines interconnected by a switching network. Some of the processing engines execute a thread. (See Vandeweerd, Abstract). Vandeweerd does not teach or suggest that which is missing from Davis, namely, defining attributes for a memory for storing messages to be operated on by a plurality of threads. Applicants contend that no conceivable combination of the cited references renders obvious Applicants' claim 1. Therefore, claims 10 and 12, which depend from claim 1, are patentable over the combination of Davis and Vandeweerd and, as such, fully satisfy the requirements of 35 U.S.C. §103. Accordingly, Applicants respectfully request that the rejection of such claims be withdrawn.

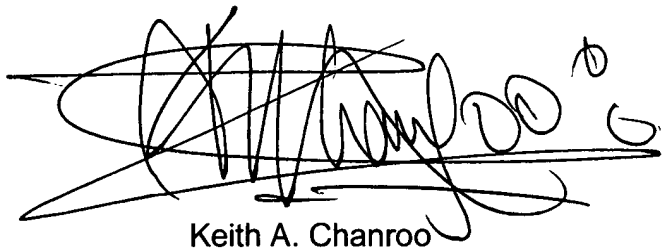
CONCLUSION

Thus, Applicants submit that none of the claims presently in the application are anticipated under the provisions of 35 U.S.C. §102 or obvious under the provisions of 35 U.S.C. §103. Consequently, Applicants believe that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If, however, the Examiner believes that there are any unresolved issues requiring any adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Keith A. Chanroo at (408) 879-7710 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

Respectfully submitted,



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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on August 18, 2006.

Pat Tompkins
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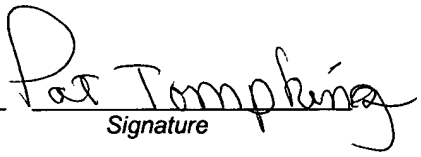

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